UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/828,862 | 04/10/2001 | Kiyotaka Imai | 99600-1 DIV | 7814 |

21254 7590 09/24/2003

MCGINN & GIBB, PLLC
8321 OLD COURTHOUSE ROAD
SUITE 200
VIENNA, VA 22182-3817

| EXAMINER | |
|---|---|
| VU, QUANG D | |
| ART UNIT | PAPER NUMBER |
| 2811 | |

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/828,862 | IMAI, KIYOTAKA | |
| | Examiner | Art Unit | |
| | Quang D Vu | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *amendment filed on07/21/03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *3-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Pri rity under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Objections*

Claim 14 is objected to because of the following informalities: In line 1, the phrase "the method as defined in claim 1" fails to clarify the subject matter of the claimed invention. Claim 1 has been canceled. Claim 14 is depended on claim 1. Claim 14 contradicts with claim 1. Appropriate correction is required.

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 3-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent No. 5,880,500 to Iwata et al.

Regarding claim 3, Iwata et al. (figure 1) teach a method for manufacturing a semiconductor device. It comprises the steps of:

implanting arsenic ions in a semiconductor substrate (100) at a first acceleration energy level (column 11, lines 8-15);

implanting phosphorous ions at a second acceleration energy level (column 10, line 66 – column 11, line 3) lower than the first acceleration energy level, a phosphorous ion implanted region (105) extending beyond the arsenic ion implanted region (108); and

performing a heat treatment to active the arsenic ions and the phosphorous ions in the ion-implanted regions to form source/drain regions and buffer regions, the buffer regions comprising phosphorous ions and extending beyond the source/drain regions (column 10, line 66 – column 12, line 45).

It is inherent that the arsenic ion implanted regions suppress a reverse channel effect in the NMOSFET.

Since first acceleration energy level (50 keV) of the arsenic ions is greater than the second acceleration energy level (30keV) of the phosphorous ions, the concentration peak of the phosphorous ions would locate in the arsenic ion implanted regions.

Iwata et al. differ from the claimed invention by not showing implanting phosphorous ions in the arsenic ion implanted regions, following the arsenic ion implanting. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the order of forming. See Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claim 4, Iwata et al. teach implanting n-type impurities in the substrate to form an n-type extension region (impurity diffusion region [107]) before the arsenic and phosphorous implanting (column 10, lines 53 – 65).

Regarding claim 5, Iwata et al. teach an acceleration energy and a dosage of the phosphorous ion are determined such that an ion-implanted region (105) of the phosphorous ion extends beyond a bottom surface of an ion-implanted region (108) of the arsenic ion. It is inherent that a dosage of the arsenic ion is determined to obtain desired electrical characteristics for the semiconductor device.

Regarding claim 6, Iwata et al. differ from the claimed invention by not showing the acceleration energy of the arsenic ion is not higher than 15 keV, and the acceleration energy of the phosphorous ion is not higher than 10 keV. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the acceleration energy of the arsenic ion is not higher than 15 keV, and the acceleration energy of the phosphorous ion is not higher than 10 keV, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 7, Iwata et al. differ from the claimed invention by not showing the dosage of the arsenic ion is between $2 \times 10^{15}/\ cm^2$ and $1 \times 10^{16}/\ cm^2$, and the dosage of the phosphorous ion is between $5 \times 10^{14}/\ cm^2$ and $2 \times 10^{15}/\ cm^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the dosage of the arsenic ion is between $2 \times 10^{15}/\ cm^2$ and $1 \times 10^{16}/\ cm^2$, and the dosage of the phosphorous ion is between $5 \times 10^{14}/\ cm^2$ and $2 \times 10^{15}/\ cm^2$, since it has been held that where the general conditions of a

claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 8, Iwata et al. (figure 1) teach a method for manufacturing a semiconductor device comprising:

implanting arsenic ions in a semiconductor substrate (100) at a first acceleration energy level to form an arsenic ion implanted region (108) (column 11, lines 8-15);

implanting phosphorous ions in the arsenic ion implanted region (impurity diffusion region [108]) at a second acceleration energy level (column 10, line 66 – column 11, line 3) lower than the first acceleration energy level; and

performing a heat treatment to activate the arsenic ions and phosphorous ions to form an n-type source/drain main region (108) comprising arsenic and phosphorous ions (column 11, line 59 – column 12, line 45), and an n-type source/drain buffer region (105) comprising phosphorous ions, the n-type source/drain buffer region (105) extending beyond the n-type source/drain main region (108).

Iwata et al. differ from the claimed invention by not showing after the implanting the arsenic ions, implanting phosphorous ions in the arsenic ion implanted regions. It would have been obvious to one having ordinary skill in the art at the time the invention was made to select the order of forming. See Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946)

(selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

Regarding claim 9, Iwata et al. teach the device comprises an n-type metal oxide semiconductor field effect transistor (NMOSFET).

Regarding claim 10, Iwata et al. teach the NMOSFET comprises a gate electrode (102) formed over a channel region (106), and wherein the n-type source/drain buffer region (105) separates the n-type source/drain main region (108) from the channel region (106).

Regarding claim 11, Iwata et al. differ from the claimed invention by not showing the substrate comprises monocrystalline silicon. It would have been obvious to one having ordinary skill in the art at the time the invention was made for the substrate comprises monocrystalline silicon because it has high electron mobility of device.

Since the arsenic ions are doped into the monocrystalline silicon substrate, the arsenic ion implanted region inherently comprises an amorphous silicon region.

Regarding claim 12, Iwata et al. teach a p-n junction formed at a first interface between the channel region (106) and the buffer region (105) is separated from a second interface between the amorphous silicon region (108) and the monocrystalline silicon.

Regarding claim 13, it is inherent that point defects generated by the implanting phosphorous ions are absorbed by the amorphous silicon, such that diffusion of the phosphorous ions during the heat-treating is suppressed.

Regarding claims 14 and 15, Iwata et al. differ from the claim invention by not showing the first acceleration energy level comprises about 10 keV or less. It would have been obvious to

one having ordinary skill in the art at the time the invention was made for the first acceleration energy level comprises about 10 keV or less, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding claim 16, Iwata et al. teach the heat-treating step comprises heat-treating at about $1000^0$ C for about 10 seconds (column 12, line 41).

Regarding claim 17, Iwata et al. differ from the claimed invention by not showing an arsenic concentration in the n-type source/drain main region is between $1x10^{20}/cm^2$ and $5x10^{21}/cm^2$ and a phosphorous concentration in the n-type source/drain buffer region is between $1x10^{18}/cm^2$ and $5x10^{19}/cm^2$. It would have been obvious to one having ordinary skill in the art at the time the invention was made for an arsenic concentration in the n-type source/drain main region is between $1x10^{20}/cm^2$ and $5x10^{21}/cm^2$ and a phosphorous concentration in the n-type source/drain buffer region is between $1x10^{18}/cm^2$ and $5x10^{19}/cm^2$, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involve only routine skill in the art. In re Aller, 105 USPQ 233.

***Response to Arguments***

Applicant's arguments with respect to claims 3-17 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quang D Vu whose telephone number is 703-305-3826. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

qv
September 17, 2003

Sara Crane
Primary Examiner